WHAT IS CLAIMED IS:

1. A method of fabricating a transistor, comprising:

providing a substrate comprising an isolation region and an active region;

forming a first doped region in the active region of the substrate with a first plurality of ions;

driving in the ions of the first doped region further into the substrate to enlarge the first doped region and to make boundaries of the first doped region graded;

forming a gate electrode over the substrate after the driving in step, wherein at least part of the gate electrode is located in the active region, and wherein at least part of the gate electrode extends over a part of the first doped region;

forming a spacer along edges of the gate electrode to form an intermediate structure;

forming a second doped region with a second plurality of ions within the first doped region, wherein a gate-side boundary of the second doped region is separated from a closest edge of the gate electrode by a first spaced distance, wherein the gate-side boundary of the second doped region is separated from a closest edge of the spacer by a second spaced distance, the second spaced distance being less than the first spaced distance.

2. The method of claim 1, further comprising:

forming a first patterned mask layer over the substrate, wherein the first patterned mask layer has a first opening formed therein at a first location in the active region, wherein the forming of the first doped region comprises implanting the first plurality of ions into the substrate at the first location through the first opening; and

removing the first patterned mask layer.

3. The method of claim 2, further comprising:

forming a second patterned mask layer over the intermediate structure, wherein the second patterned mask layer has a second opening formed therein at a second location in the active region, and wherein the second location is located within the first location, wherein the forming of the second doped region comprises implanting the second plurality of ions into the substrate at the second location through the second opening, and wherein the second opening is not aligned with the closest edge of the spacer; and

removing the second patterned mask layer.

4. The method of claim 1, further comprising:

implanting a third plurality of ions into the substrate at the active region in alignment with the edges of the gate electrode and edges of the isolation region to form a lightly doped region, wherein the spacer extends over part of the lightly doped region.

5. The method of claim 1, wherein the driving in step is performed at a temperature between about 1000 and about 1200° C.

6. The method of claim 1, wherein the isolation region has a field oxide structure.

7. The method of claim 1, wherein the isolation region has a shallow trench filled with insulating material.

8. The method of claim 2, wherein the removing of the first patterned mask layer occurs before the driving in step.

9. The method of claim 2, wherein the removing of the first patterned mask layer occurs after the driving in step.

10. The method of claim 2, wherein the removing of the first patterned mask layer occurs during the driving in step.

11. The method of claim 2, wherein the first patterned mask layer comprises photoresist material.

12. The method of claim 3, wherein the second patterned mask layer comprises photoresist material.

13. The method of claim 1, wherein an isolation-side boundary of the second doped region is separated from a closest edge of the isolation region by a third spaced distance.

14. The method of claim 13, wherein the third spaced distance is about equal in length to the first spaced distance.

15. A method of fabricating a transistor, comprising:

providing a substrate;

defining an active region, wherein at least part of the active region extends into the substrate;

forming an isolation region, wherein at least a majority of the isolation region extends at least partially around the active region, and wherein the isolation region comprises an insulating material formed at least partially in the substrate;

forming a first patterned mask layer over the substrate, wherein the first patterned mask layer has a first opening formed therein at a first location in the active region;

implanting a first plurality of ions into the substrate at the first location through the first opening to form a first doped region;

removing the first patterned mask layer;

driving in the implanted ions of the first doped region further into the substrate to enlarge the first doped region and to make boundaries of the first doped region graded;

forming a gate electrode over the substrate after the driving in step, wherein at least part of the gate electrode is located in the active region, and wherein at least part of the gate electrode extends over a part of the first doped region;

forming a spacer along edges of the gate electrode to form an intermediate structure;

forming a second patterned mask layer over the intermediate structure, wherein the second patterned mask layer has a second opening formed therein at a second location in the active region, and wherein the second location is located within the first location;

implanting a second plurality of ions into the substrate at the second location through the second opening to form a second doped region within the first doped region, wherein a gate-side

boundary of the second doped region is separated from a closest edge of the gate electrode by a first spaced distance, wherein the gate-side boundary of the second doped region is separated from a closest edge of the spacer by a second spaced distance, the second spaced distance being less than the first spaced distance, and wherein the second opening is not aligned with the closest edge of the spacer.

16. The method of claim 15, further comprising:

implanting a third plurality of ions into the substrate at the active region in alignment with the edges of the gate electrode and edges of the isolation region to form a lightly doped region, wherein the spacer extends over part of the lightly doped region;

17. The method of claim 15, wherein the forming of the isolation region is performed before the forming of the first patterned mask layer.

18. The method of claim 15, wherein the forming of the isolation region is performed after the driving in step.

19. A semiconductor device, comprising:

a substrate;

a volume defined as being an active region, wherein at least part of the active region extends into the substrate;

a gate electrode formed over the substrate, wherein at least part of the gate electrode is located in the active region;

a spacer formed along edges of the gate electrode;

a driven-in first doped region formed in the substrate, wherein boundaries of the first doped region are graded, and wherein a gate-side boundary of the first doped region extends laterally below part of the gate electrode; and

a second doped region formed within the first doped region, wherein a gate-side boundary of the second doped region is separated from a closest edge of the gate electrode by a first spaced distance, wherein the gate-side boundary of the second doped region is separated from a closest edge of the spacer by a second spaced distance, and wherein the first spaced distance is greater than the second spaced distance.

20. The semiconductor device of claim 19, further comprising a shallow trench isolation region comprising an insulating material formed at least partially in the substrate, wherein at least a majority of the isolation region extends at least partially around the active region.

21. The semiconductor device of claim 19, further comprising an isolation region comprising an insulating material formed at least partially in the substrate, wherein at least a majority of the isolation region extends at least partially around the active region, wherein the isolation region has a field oxide structure.

22. The semiconductor device of claim 19, further comprising an isolation region comprising an insulating material formed at least partially in the substrate, wherein at least a majority of the isolation region extends at least partially around the active region, and wherein an isolation-side boundary of the second doped region is separated from a closest edge of the isolation region by a third spaced distance.

23. The semiconductor device of claim 22, wherein the third spaced distance is about equal in length to the first spaced distance.

24. The semiconductor device of claim 19, wherein the semiconductor device comprises a transistor having a breakdown voltage equal to or greater than about 30 volts.

25. A semiconductor device, comprising:

a transistor comprising

a gate electrode;

a spacer formed along edges of the gate electrode, the spacer having an outer edge; and

a drain region comprising

a first doped region, wherein at least part of the first doped region is underlying at least part of the gate electrode, and

a second doped region formed in the first doped region and spaced from the gate electrode a greater distance than from the outer edge of the spacer.

26. The semiconductor device of claim 25, wherein the transistor is a high voltage transistor having a breakdown voltage equal to or greater than about 30 volts.

27. The semiconductor device of claim 25, wherein the first doped region is formed in a well of opposite doping type and wherein a depletion region between the first doped region and the well has a width between about 0.8 μm and about 1.0 μm when a bias of about 12 volts is applied.

28. A semiconductor device, comprising:

a high voltage transistor having a breakdown voltage equal to or greater than about 30 volts, the transistor comprising

a gate electrode;

a spacer formed along edges of the gate electrode, the spacer having an outer edge;

a well region; and

a drain region comprising

a first doped region formed in the well region, wherein at least part of the first doped region is underlying at least part of the gate electrode, wherein the first doped region has an opposite doping type than the well region, and wherein a depletion region between the first doped region and the well has a width between about 0.8 μm and about 1.0 μm when a bias of about 12 volts is applied, and

a second doped region formed in the first doped region and spaced from the gate electrode a greater distance than from the outer edge of the spacer.